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HP E2473A Intel i960H-Series Preprocessor Interface

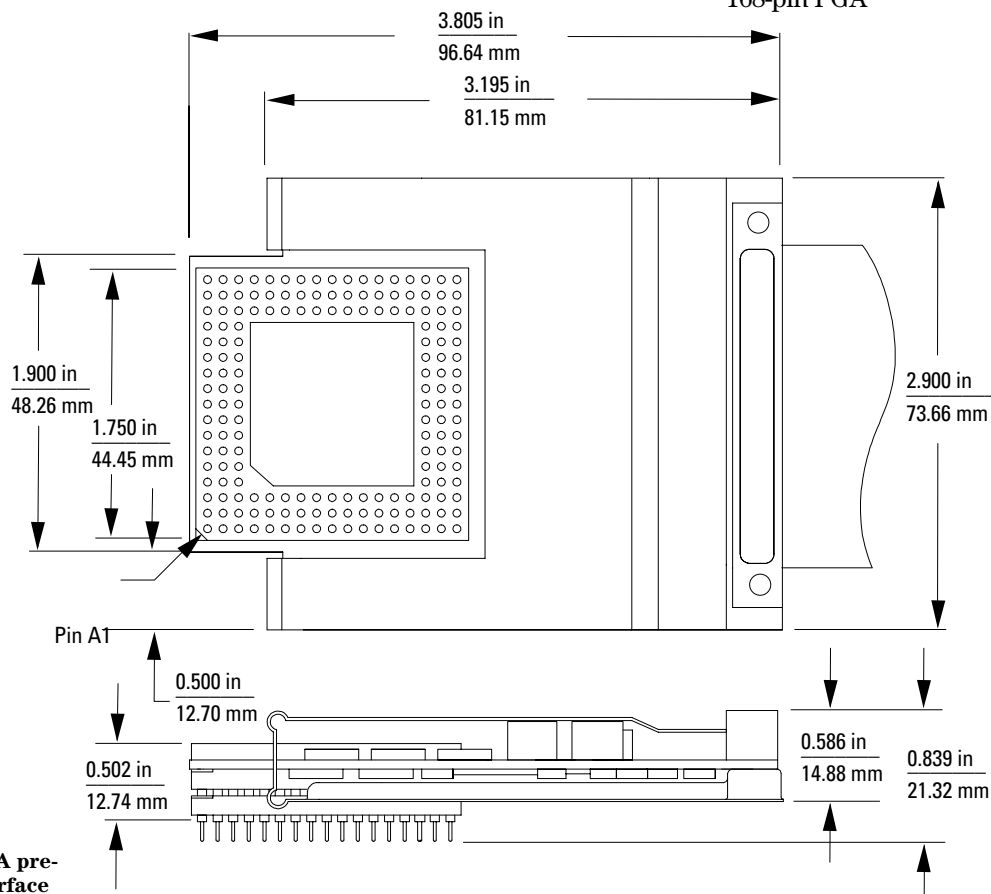
For use with HP logic analyzers

The HP E2473A preprocessor for the Intel i960H-series is a mechanical and electrical interface between the Intel i960H-series and various HP logic analyzers for real-time state analysis. The preprocessor routes signals, aligns address, data and status signals, and filters non-data transfers such as idle and wait states.

Preprocessor software configures the logic analyzer labeling address, data and status lines. Additionally, when a state trace is displayed, i960 mnemonics are listed providing data captured and the controlling program.

Microprocessors Supported
Intel 80960HA, 80960HD, and 80960HT microprocessors, and all microprocessors made by other manufacturers that comply with the Intel i960H-series specification. Both 5V and 3.3V versions are supported.

Package Supported
168-pin PGA



The HP E2473A preprocessor interface

Capabilities

- The HP E2473A preprocessor supports timing, state-per-clock, and state-per-transfer operating modes. While in timing mode, the HP E2473A buffers i960H-series signals and passes them to the logic analyzer. In state-per-clock mode all valid data transfers on the i960H-series bus clock data into the logic analyzer. State-per-transfer mode aligns address, status, and data, before clocking the logic analyzer, deskewing the pipelined bus of the i960H-series processor.
- The HP E2473A filters states so that only valid data transfers (instruction fetches/caches fills, data reads and writes) get clocked into the analyzer. Wait states, idle states (that is, states when there is no valid data on the bus) do not get passed to the analyzer. This ensures optimal use of the analyzer's acquisition memory. Logic analyzer time tags can be used to measure the duration of the transactions from state to state.
- The following i960 instructions can be selected to be displayed or suppressed: unexecuted prefetches, jumps, calls/returns, and other instructions. In addition, memory read/write cycles can be displayed or suppressed.
- Monitors all i960H-series signals of interest including the on-chip interrupt and DMA controllers.

Logic Analyzers Supported

- HP 1660A/AS, C/CS
- HP 1661A/AS, C/CS
- HP 1670A
- HP 1671A
- HP 16550A (one or two cards)
- HP 16554A/55A/56A (two cards)

Probes Required

- Six 17-channel pods are required for inverse assembly
- Seven 17-channel pods are required to monitor all i960 signals

Electrical Characteristics

Power Requirements

All power is supplied by the logic analyzer.

Microprocessor Clock Speed

- 40 MHz with 1X core (40 MHz internal)
- 33 MHz with 2X core (66 MHz internal)
- 25 MHz with 3X core (75 MHz internal)
- Minimum microprocessor bus clock speed supported is 5 MHz

Timing Analysis

The following signals have 1 ns channel-to-channel skew in timing analysis: DATA[31:0], BTERM#, BLAST#, RESET#, WAIT, NMI, ONCE#, HOLD, HOLDA, BOFF#, BREQ, BSTALL, FAIL#, READY#, STEST, PCHK#, DP[3:0], XINT[7:0], DT/R#, DEN#, VOLDET, TRST#, TDI, TDO, TMS.

The following signals are sampled only once (in state and timing mode) for each rising edge of the CPU clock: A[31:0], W/R#, D/C#, SUP#, ADS#, LOCK#, BE#[3:0], CT[3:0].

Signal Line Loading

- Approximately 16 pF on ADS#, RESET#, BLAST#, A2, CT0, CT1, READY#, BTERM#, WAIT#, and BE[2:0].
- Approximately 8 pF on all other signals.

Environmental Characteristics

Temperature

Operation 0 to +50 °C

+32 to +131 °F

Altitude 4,600 m 50,000 feet

Humidity Up to 75% noncondensing. Avoid sudden, extreme temperature changes which could cause condensation on the circuit board.

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